



ORDERING INFORMATION		
Temp Range	Package	Part Number
DG411/DG412		
- 40 to 85 °C	16-Pin Plastic DIP	DG411DJ DG411DJ-E3
- 40 to 85 °C		16-Pin Narrow SOIC
	DG411DY DG411DY-E3 DG411DY-T1 DG411DY-T1-E3	
		DG412DY DG412DY-E3 DG412DY-T1 DG412DY-T1-E3
DG413		
- 40 to 85 °C	16-Pin Plastic DIP	DG413DJ DG413DJ-E3
	16-Pin Narrow SOIC	DG413DY DG413DY-E3 DG413DY-T1 DG413DY-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter	Limit	Unit	
V+ to V-	44	V	
GND to V-	25		
V _L	(GND - 0.3) to (V+) + 0.3		
Digital Inputs ^a , V _S , V _D	(V-) -2 to (V+) + 2 or 30 mA, whichever occurs first		
Continuous Current (Any Terminal)	30	mA	
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle)	100		
Storage Temperature	(AK, AZ Suffix)	- 65 to 150	°C
	(DJ, DY Suffix)	- 65 to 125	
Power Dissipation (Package) ^b	16-Pin Plastic DIP ^c	470	mW
	16-Pin Narrow SOIC ^d	600	
	16-Pin CerDIP ^e	900	
	LCC-20 ^e	900	

Notes:

- a. Signals on S_x, D_x, or IN_x exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6 mW/°C above 25 °C.
- d. Derate 7.6 mW/°C above 75 °C.
- e. Derate 12 mW/°C above 75 °C.



SPECIFICATIONS ^a									
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 15 V, V ₋ = - 15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix - 55 to 125 °C		D Suffix - 40 to 85 °C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	r _{DS(on)}	V ₊ = 13.5 V, V ₋ = - 13.5 V I _S = - 10 mA, V _D = ± 8.5 V	Room Full	25		35 45		35 45	Ω
Switch Off Leakage Current	I _{S(off)}	V ₊ = 16.5 V, V ₋ = - 16.5 V V _D = ± 15.5 V, V _S = ± 15.5 V	Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	nA
	I _{D(off)}		Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	
Channel On Leakage Current	I _{D(on)}	V ₊ = 16.5 V, V ₋ = - 16.5 V V _S = V _D = ± 15.5 V	Room Full	± 0.1	- 0.4 - 40	0.4 40	- 0.4 - 10	0.4 10	
Digital Control									
Input Current, V _{IN} Low	I _{IL}	V _{IN} under test = 0.8 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	μA
Input Current, V _{IN} High	I _{IH}	V _{IN} under test = 2.4 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	
Dynamic Characteristics									
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _S = ± 10 V, See Figure 2	Room Full	110		175 240		175 220	ns
Turn-Off Time	t _{OFF}		Room Full	100		145 160		145 160	
Break-Before-Make Time Delay	t _D	DG413 Only, V _S = 10 V R _L = 300 Ω, C _L = 35 pF	Room	25					
Charge Injection	Q	V _g = 0 V, R _g = 0 Ω C _L = 10 nF	Room	5					pC
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room	68					dB
Channel-to-Channel Crosstalk ^e	X _{TALK}		Room	85					
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz	Room	9					pF
Drain Off Capacitance ^e	C _{D(off)}		Room	9					
Channel On Capacitance ^e	C _{D(on)}		Room	35					
Power Supplies									
Positive Supply Current	I ₊	V ₊ = 16.5 V, V ₋ = - 16.5 V V _{IN} = 0 or 5 V	Room Full	0.0001		1 5		1 5	μA
Negative Supply Current	I ₋		Room Full	- 0.0001	- 1 - 5		- 1 - 5		
Logic Supply Current	I _L		Room Full	0.0001		1 5		1 5	
Ground Current	I _{GND}		Room Full	- 0.0001	- 1 - 5		- 1 - 5		

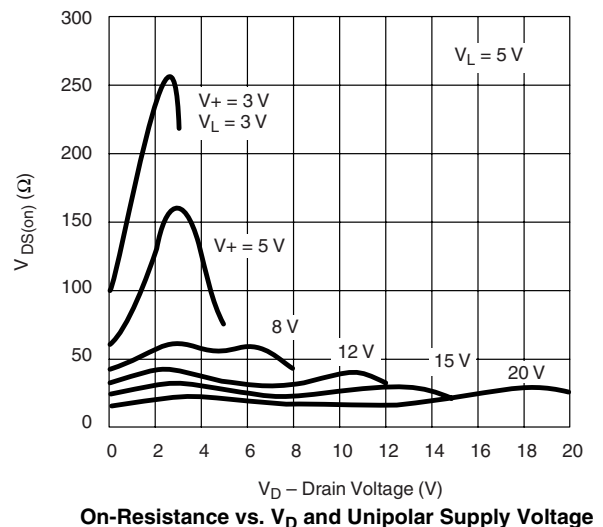
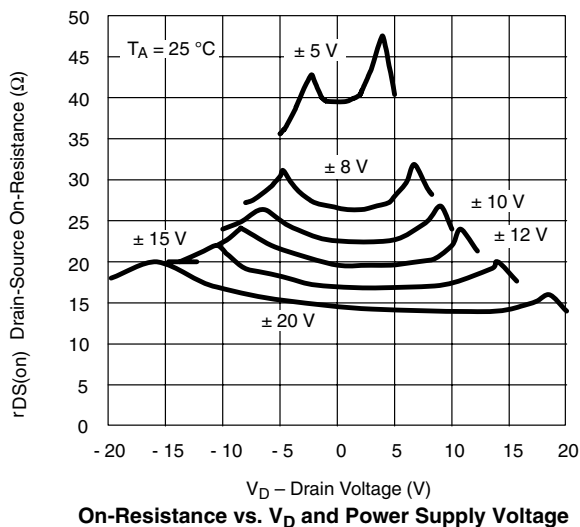
SPECIFICATIONS FOR UNIPOLAR SUPPLIES ^a									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f	Temp ^b	Typ ^c	A Suffix - 55 to 125 °C		D Suffix - 40 to 85 °C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full			12		12	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_+ = 10.8\text{ V}$, $I_S = -10\text{ mA}$, $V_D = 3\text{ V}$, 8 V	Room Full	40		80 100		80 100	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$, See Figure 2	Room Hot	175		250 400		250 315	ns
Turn-Off Time	t_{OFF}		Room Hot	95		125 140		125 140	
Break-Before-Make Time Delay	t_D	DG413 Only, $V_S = 8\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$	Room	25					
Charge Injection	Q	$V_g = 6\text{ V}$, $R_g = 0\ \Omega$, $C_L = 10\text{ nF}$	Room	25					pC
Power Supplies									
Positive Supply Current	I_+	$V_+ = 13.5\text{ V}$, $V_{IN} = 0\text{ or }5\text{ V}$	Room Hot	0.0001		1 5		1 5	μA
Negative Supply Current	I_-		Room Hot	-0.0001	-1 -5		-1 -5		
Logic Supply Current	I_L		Room Hot	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Hot	-0.0001	-1 -5		-5		

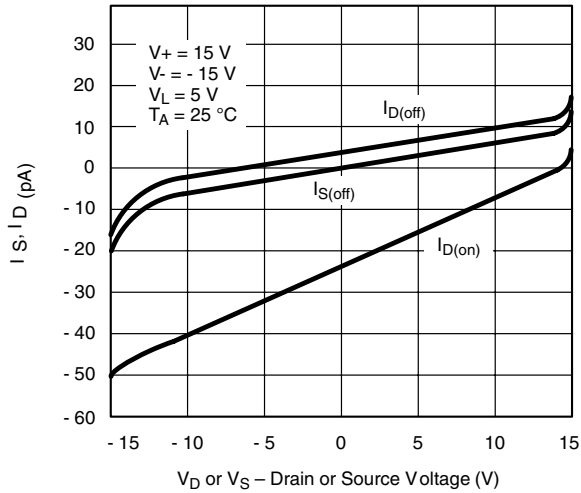
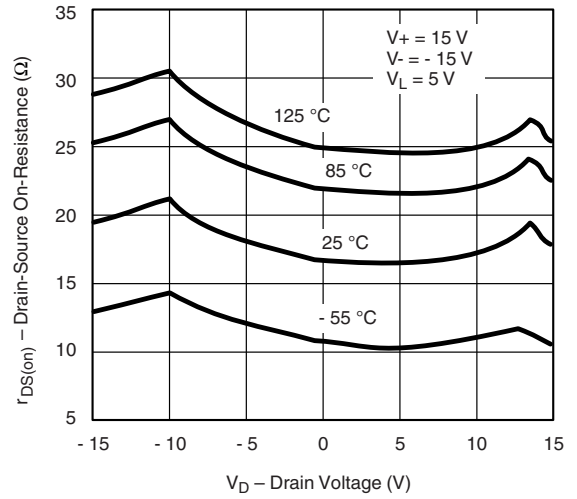
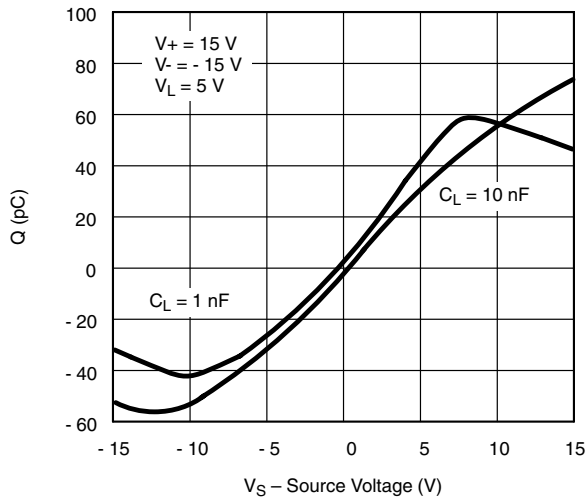
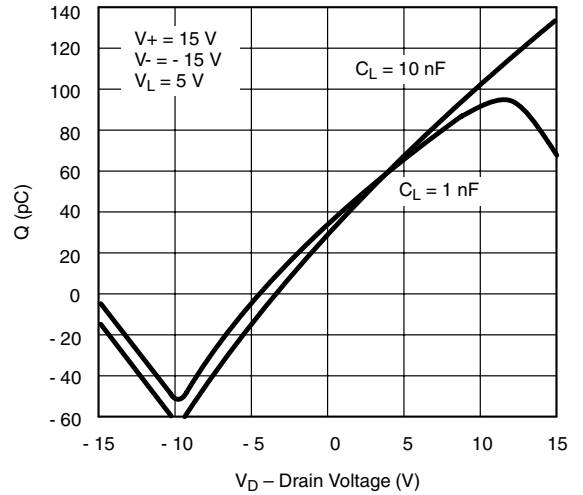
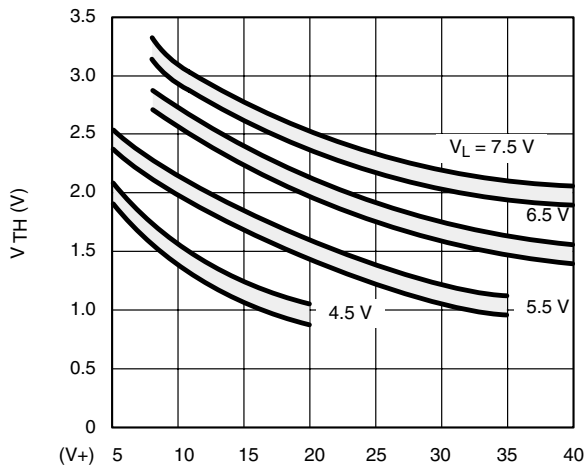
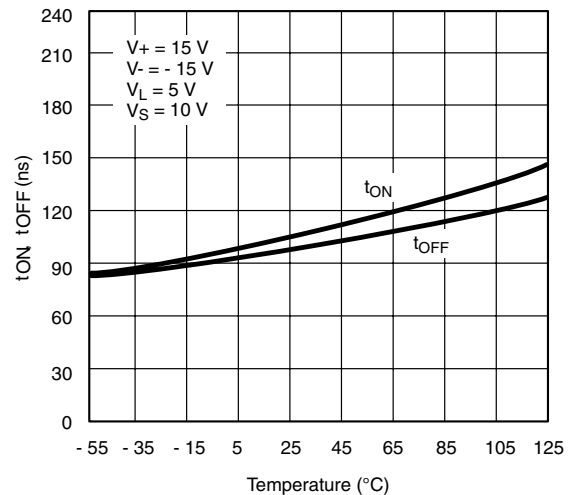
Notes:

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.

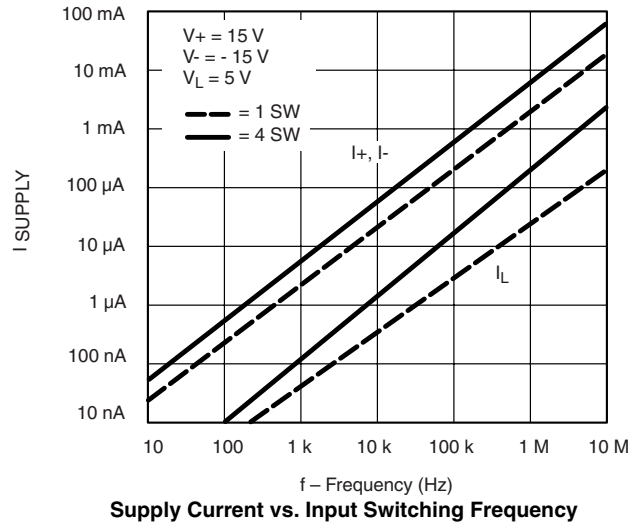
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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Leakage Current vs. Analog Voltage

 I_D, I_S Leakages vs. Temperature

Charge Injection vs. Analog Voltage

Charge Injection vs. Analog Voltage

Input Switching Threshold vs. Supply Voltage

Switching Time vs. Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

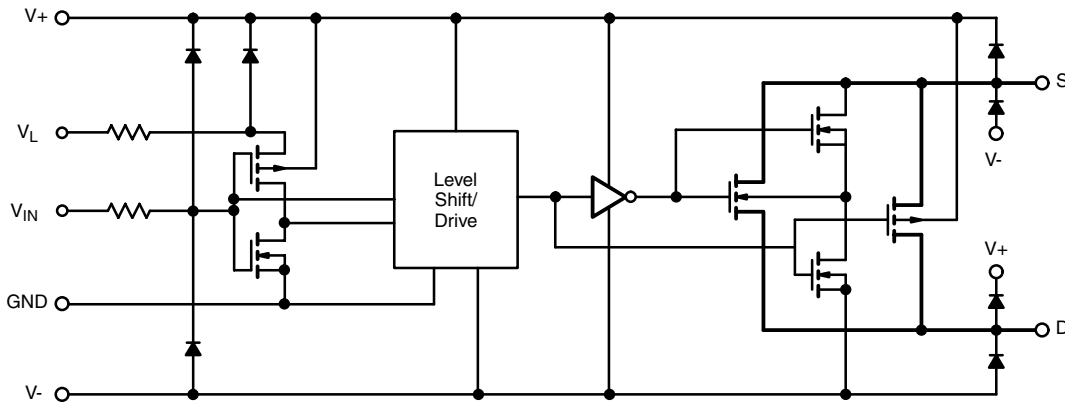
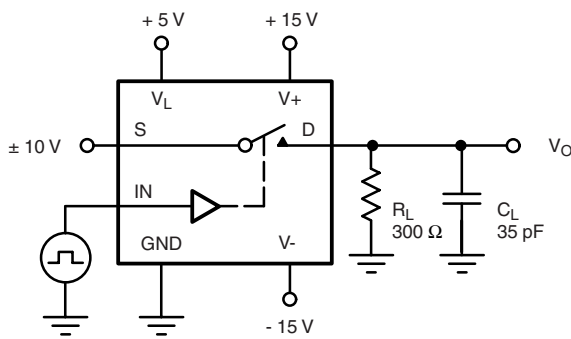


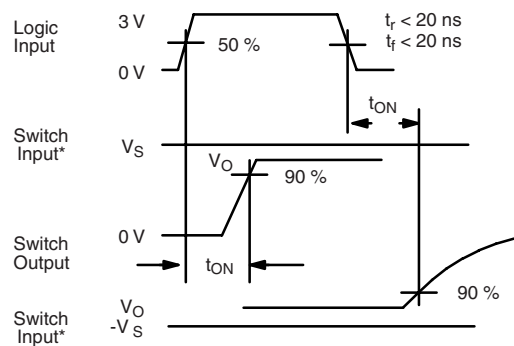
Figure 1.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



* $V_S = 10\text{ V}$ for t_{ON} , $V_S = -10\text{ V}$ for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time

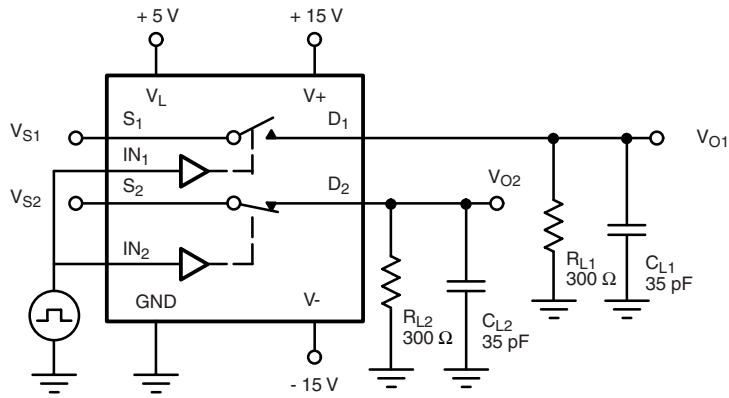
TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

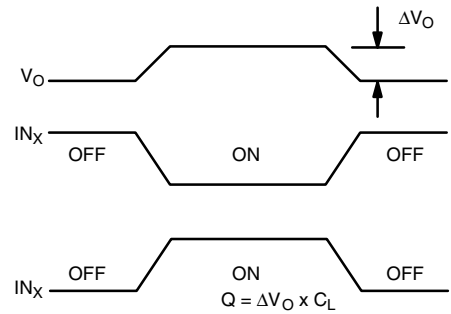
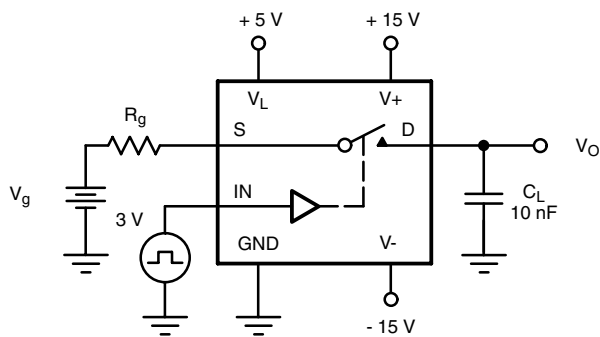
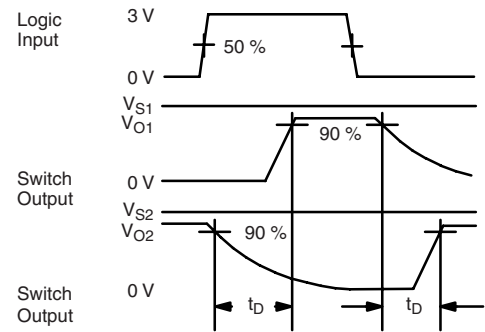
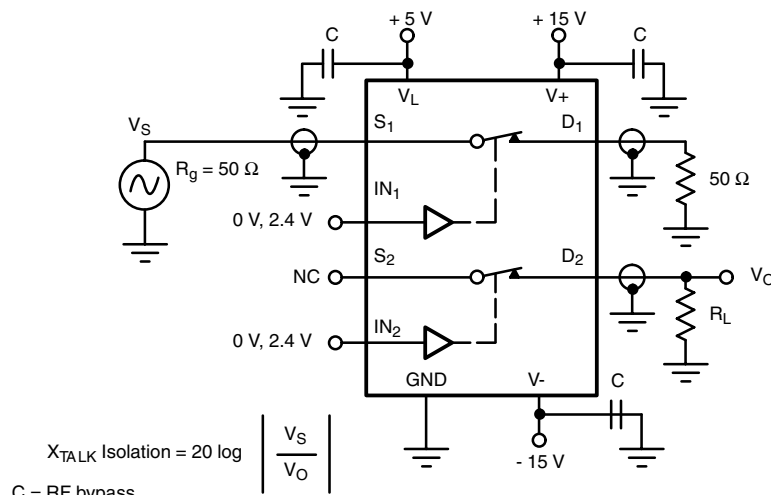
Figure 3. Break-Before-Make (DG413)

 I_{N_X} dependent on switch configuration Input polarity determined by sense of switch.

Figure 4. Charge Injection


$$X_{\text{TALK Isolation}} = 20 \log \left| \frac{V_S}{V_O} \right|$$

$C = \text{RF bypass}$

Figure 5. Crosstalk

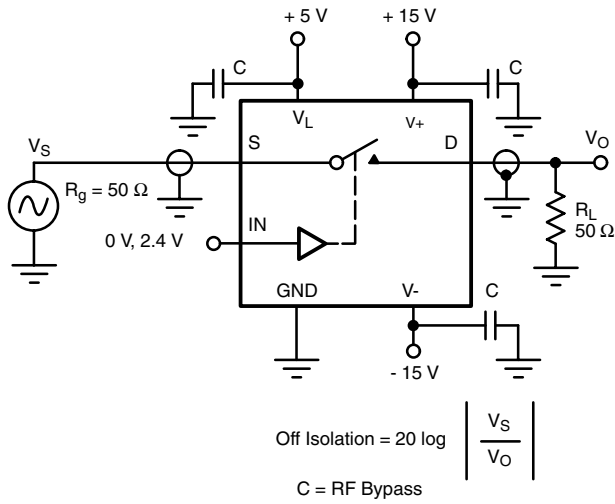


Figure 6. Off Isolation

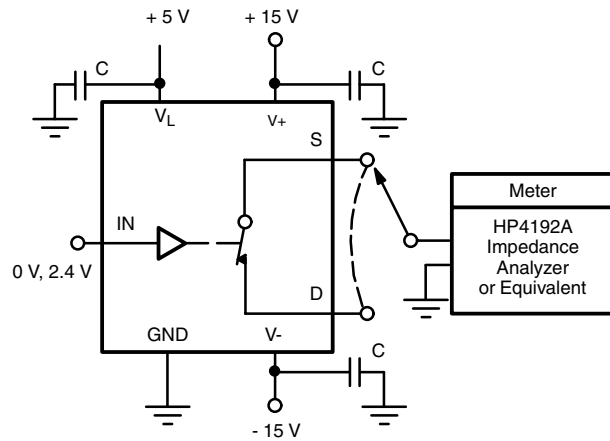


Figure 7. Source/Drain Capacitances

APPLICATIONS

Single Supply Operation:

The DG411/412/413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. In single supply operation, V+ is tied to VL and V- is tied to 0 V. See Input Switching Threshold vs. Supply Voltage curve for VL versus input threshold requirements.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 8, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

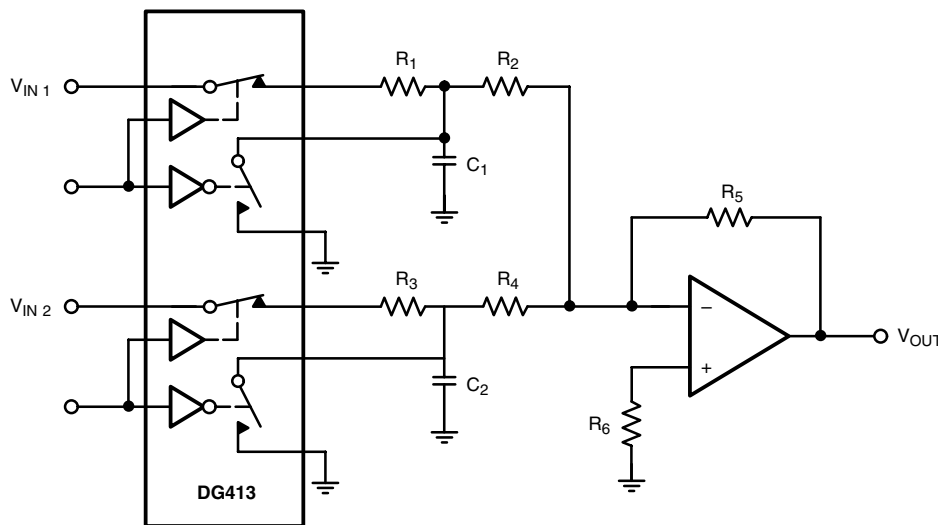


Figure 8. Summing Amplifier

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