PD - 94418

International
IOR Rectifier

IRFB20N50K

SMPS MOSFET

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	0.21Ω	20A

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

TO-220AB

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low $R_{DS(on)}$

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	20	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	12	
I_{DM}	Pulsed Drain Current ①	80	
P_D @T_C = 25°C	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	6.9	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 screw	10	N

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	330	mJ
I_{AR}	Avalanche Current①	—	20	A
E_{AR}	Repetitive Avalanche Energy①	—	28	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	58	

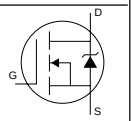
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.61	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	0.21	0.25	Ω	V_{GS} = 10V, I_D = 12A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	50	µA	V_{DS} = 500V, V_{GS} = 0V
		——	——	250	µA	V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	11	——	——	S	V_{DS} = 50V, I_D = 12A
Q_g	Total Gate Charge	——	——	110	nC	I_D = 20A
Q_{gs}	Gate-to-Source Charge	——	——	33		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	54		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	22	——	ns	V_{DD} = 250V
t_r	Rise Time	——	74	——		I_D = 20A
$t_{d(off)}$	Turn-Off Delay Time	——	45	——		R_G = 7.5Ω
t_f	Fall Time	——	33	——		V_{GS} = 10V,See Fig. 10 ④
C_{iss}	Input Capacitance	——	2870	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	320	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	34	——		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	3480	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	85	——		V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	160	——		V_{GS} = 0V, V_{DS} = 0V to 400V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	20	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	80		
V_{SD}	Diode Forward Voltage	——	——	1.5	V	T_J = 25°C, I_S = 20A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	520	780	ns	T_J = 25°C, I_F = 20A
Q_{rr}	Reverse Recovery Charge	——	5.3	8.0	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 1.6mH, R_G = 25Ω, I_{AS} = 20A,

③ I_{SD} ≤ 20A, di/dt ≤ 350A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

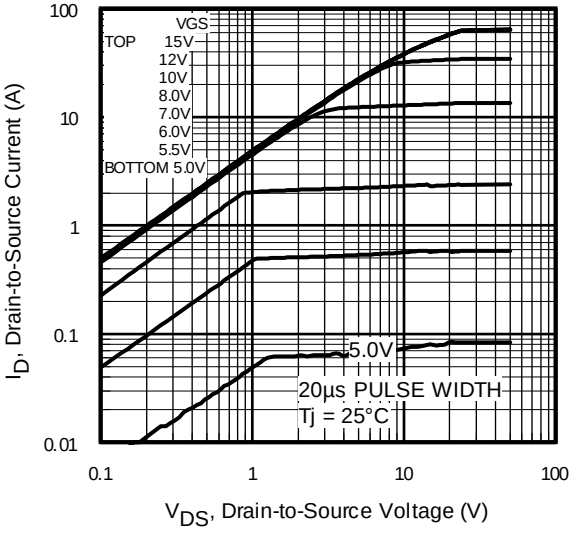


Fig 1. Typical Output Characteristics

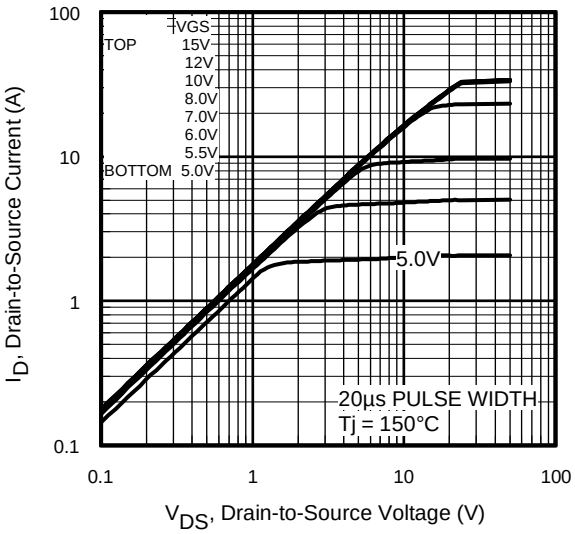


Fig 2. Typical Output Characteristics

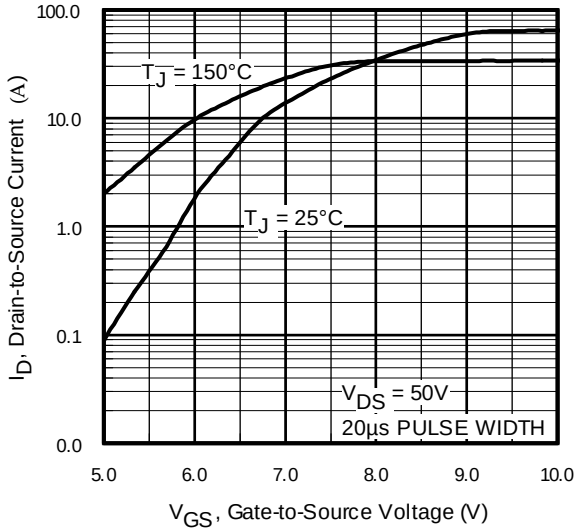


Fig 3. Typical Transfer Characteristics

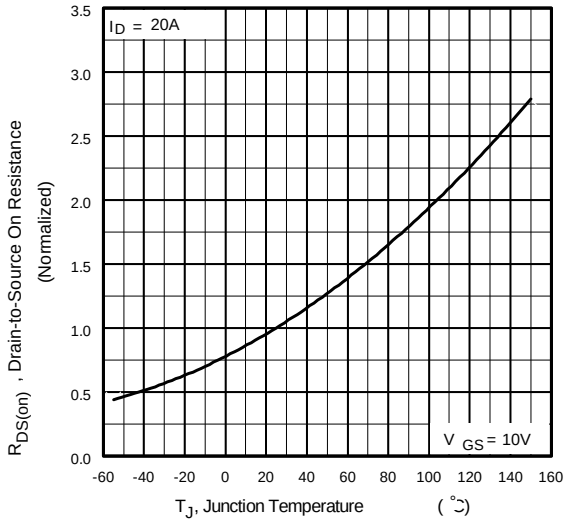


Fig 4. Normalized On-Resistance Vs. Temperature

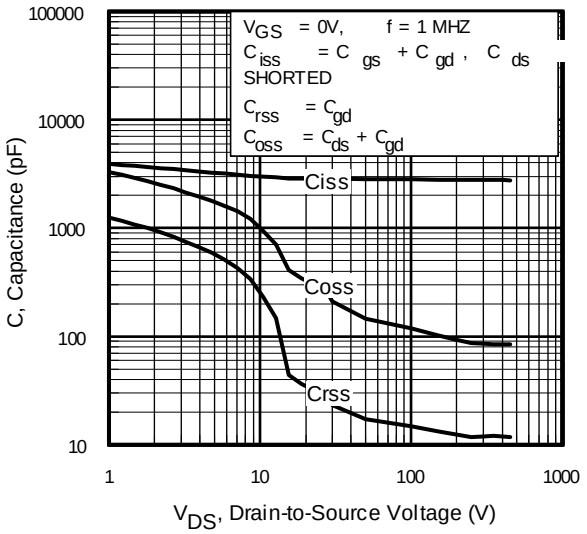


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

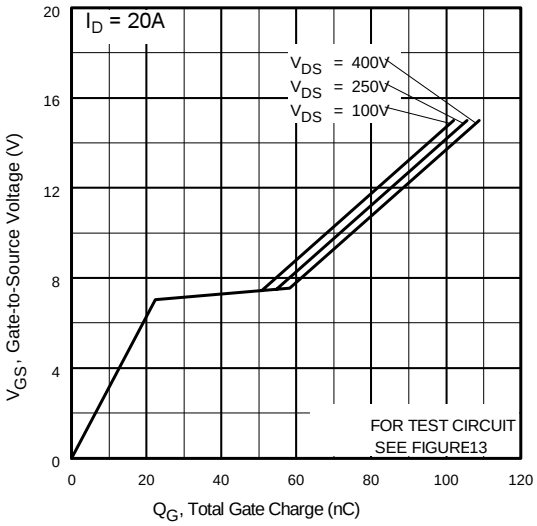


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

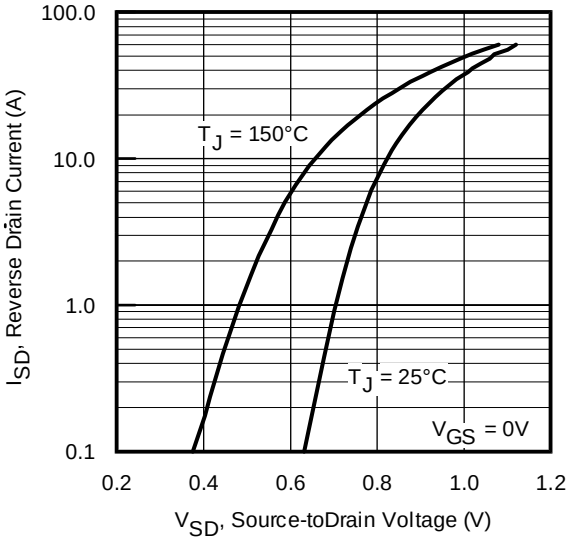


Fig 7. Typical Source-Drain Diode Forward Voltage

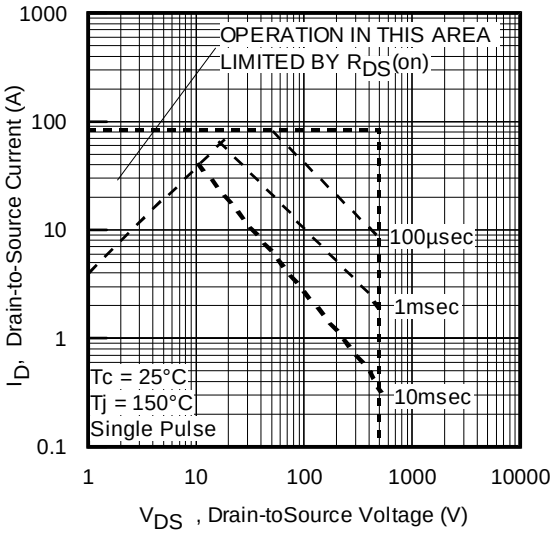


Fig 8. Maximum Safe Operating Area

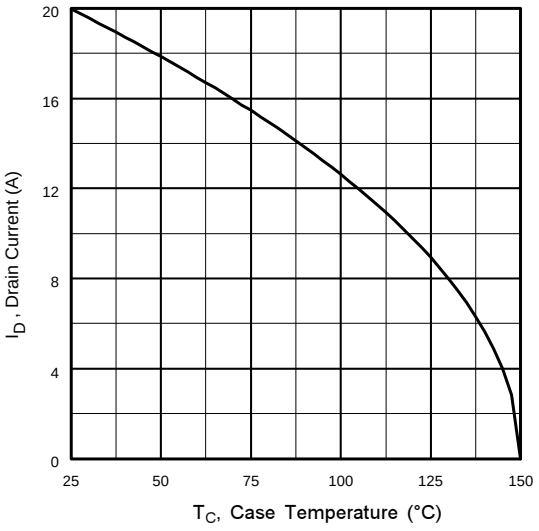


Fig 9. Maximum Drain Current Vs. Case Temperature

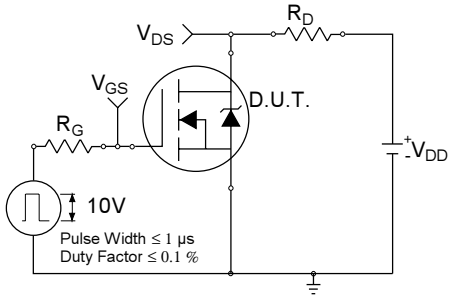


Fig 10a. Switching Time Test Circuit

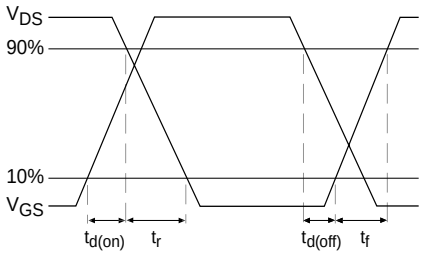


Fig 10b. Switching Time Waveforms

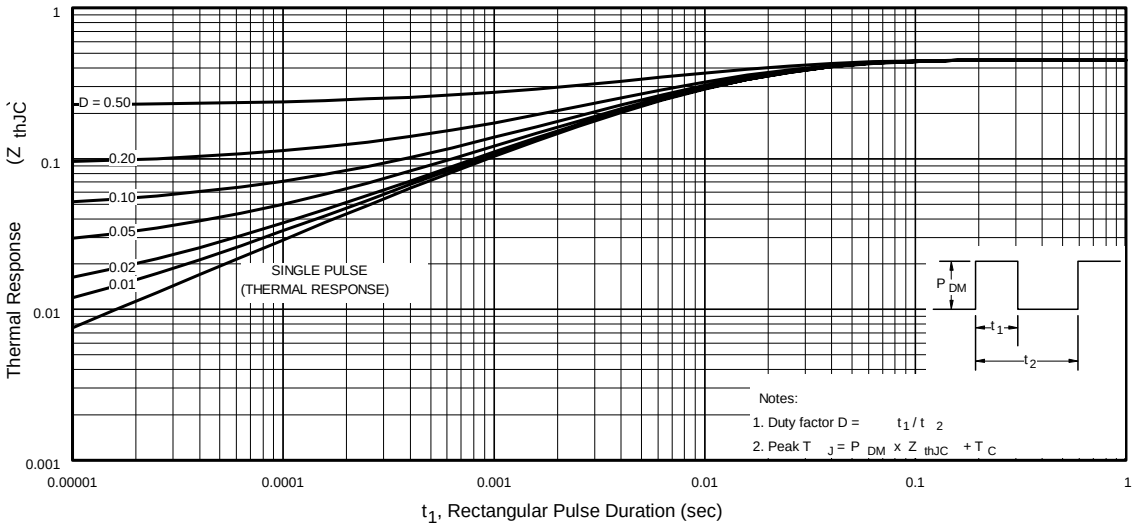


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

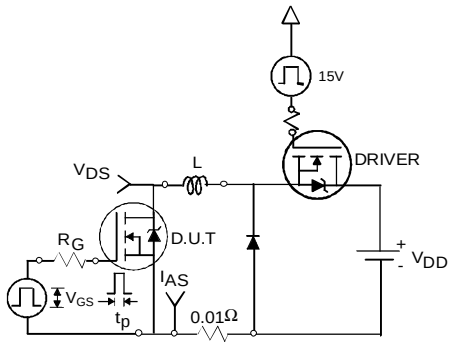


Fig 12a. Unclamped Inductive Test Circuit

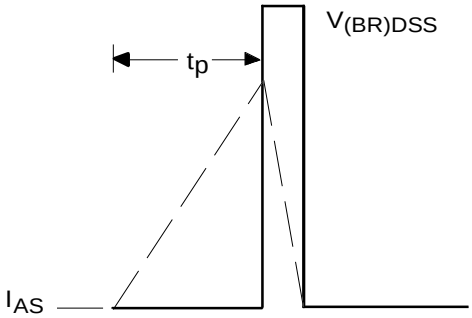


Fig 12b. Unclamped Inductive Waveforms

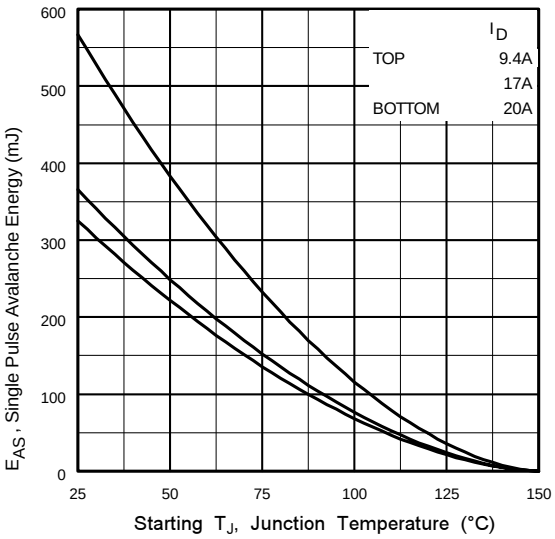


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

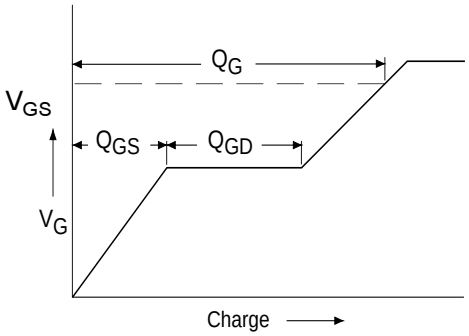


Fig 13a. Basic Gate Charge Waveform

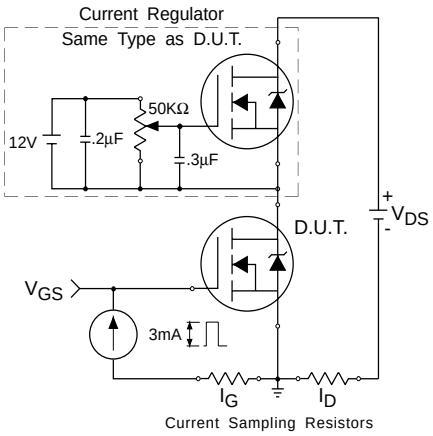
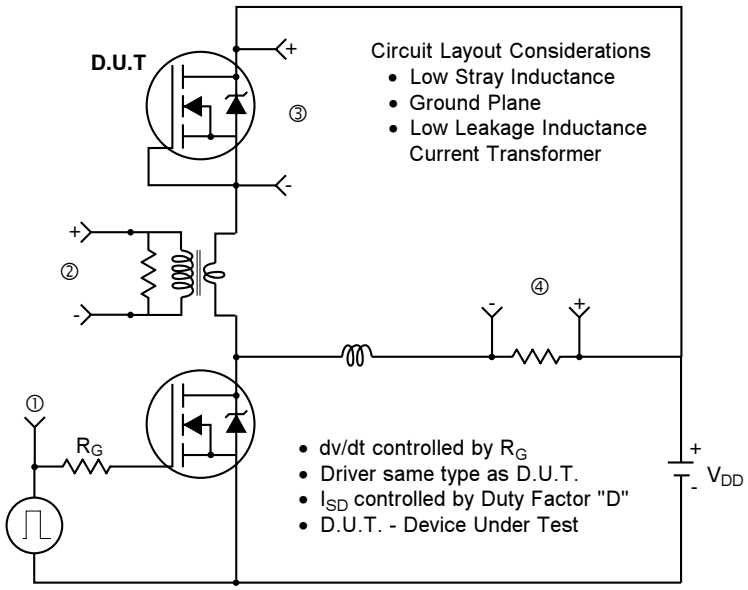
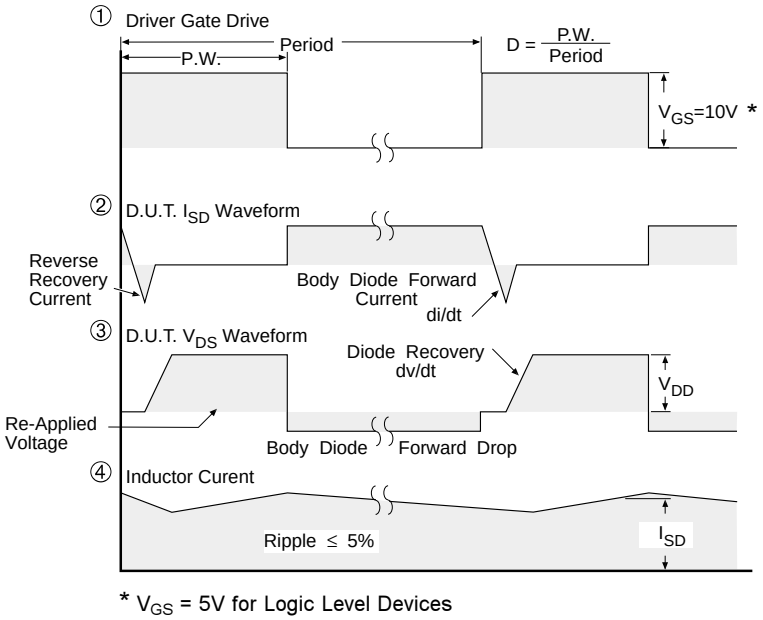


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



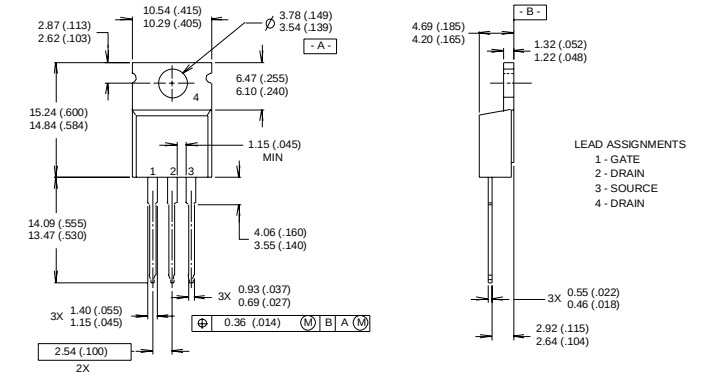


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

TO-220 Package Outline

Dimensions are shown in millimeters (inches)

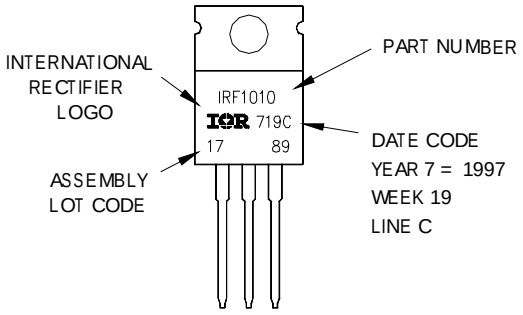


NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220 Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.4/02