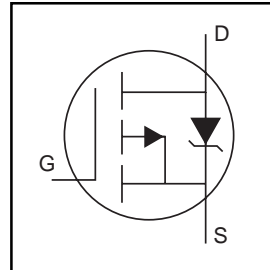


- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- P-Channel
- Fast Switching
- Fully Avalanche Rated

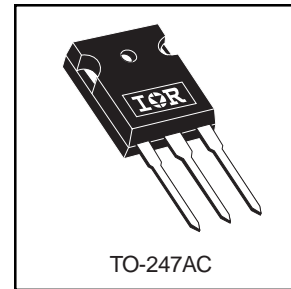


$V_{DSS} = -100V$
$R_{DS(on)} = 0.117\Omega$
$I_D = -23A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-23	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-16	
I_{DM}	Pulsed Drain Current ①⑤	-76	
$P_D @ T_C = 25^\circ C$	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	430	mJ
I_{AR}	Avalanche Current①	-11	A
E_{AR}	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

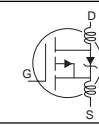
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

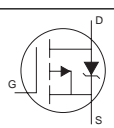
IRFP9140N

International
IR Rectifier

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.117	Ω	$V_{GS} = -10V, I_D = -13A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	5.3	—	—	S	$V_{DS} = -50V, I_D = 11A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -100V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	97	nC	$I_D = -11A$
Q_{gs}	Gate-to-Source Charge	—	—	15		$V_{DS} = -80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	51		$V_{GS} = -10V$, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = -50V$
t_r	Rise Time	—	67	—		$I_D = -11A$
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		$R_G = 5.1\Omega$
t_f	Fall Time	—	51	—		$R_D = 4.2\Omega$, See Fig. 10 ④⑤
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	400	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	240	—		$f = 1.0\text{MHz}$, See Fig. 5 ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-23	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	-76		
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	$T_J = 25^\circ\text{C}, I_S = -13A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	150	220	ns	$T_J = 25^\circ\text{C}, I_F = -11A$
Q_{rr}	Reverse Recovery Charge	—	830	1200	μC	$di/dt = -100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 7.1\text{mH}$
 $R_G = 25\Omega, I_{AS} = -11A$. (See Figure 12)

③ $I_{SD} \leq -11A, di/dt \leq -470A/\mu s, V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ Uses IRF9540N data and test conditions

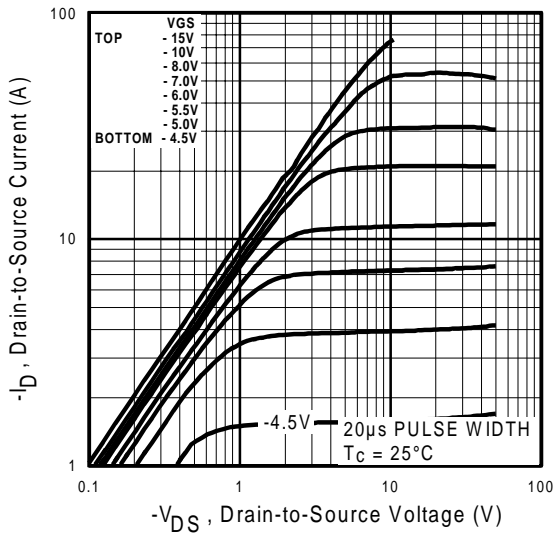


Fig 1. Typical Output Characteristics

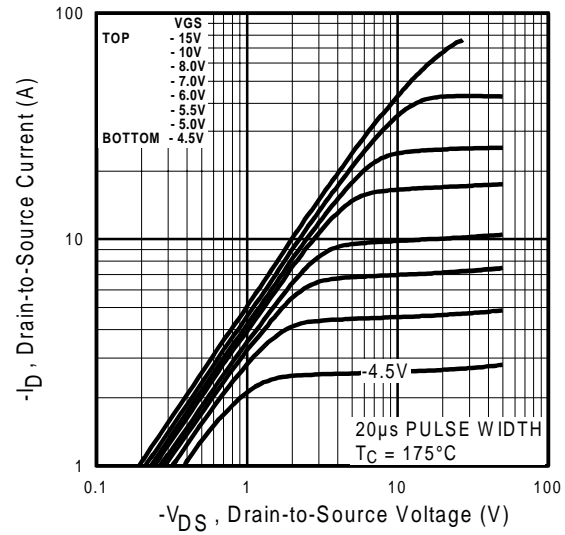


Fig 2. Typical Output Characteristics

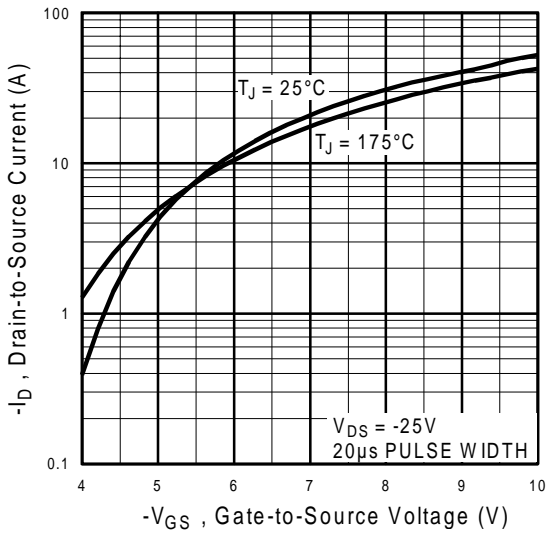


Fig 3. Typical Transfer Characteristics

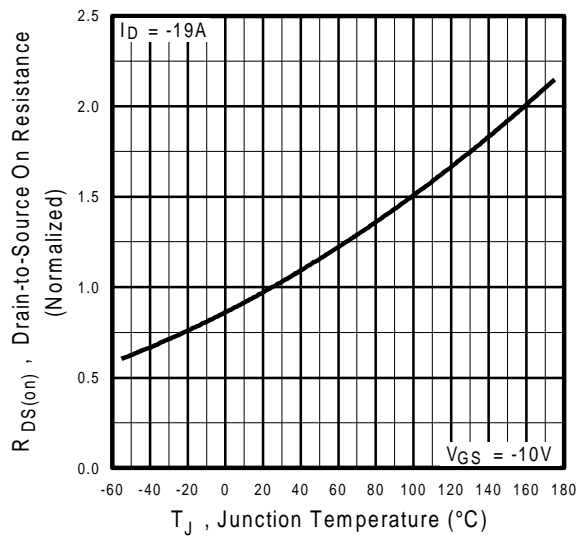


Fig 4. Normalized On-Resistance Vs. Temperature

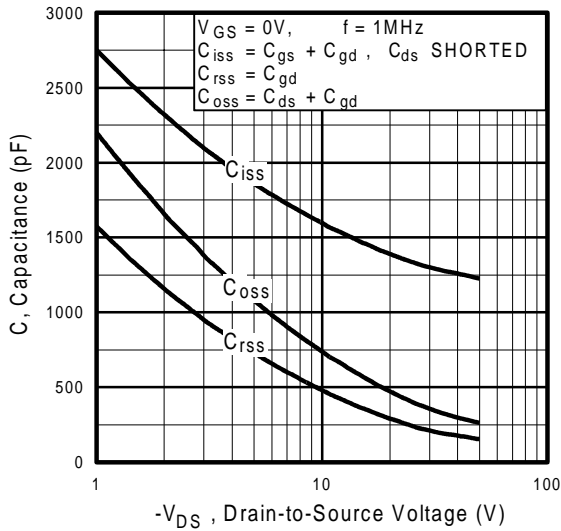


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

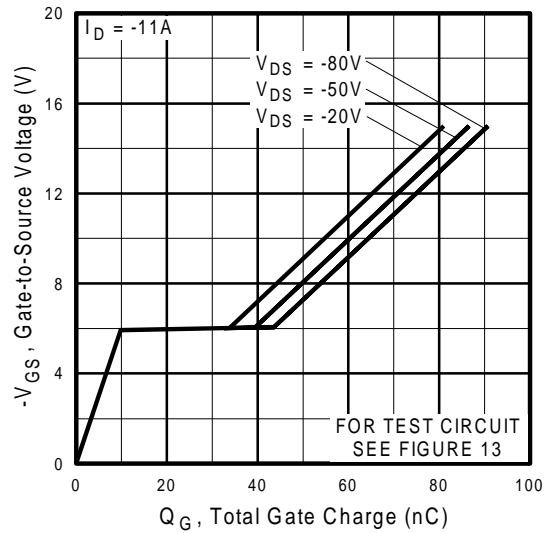


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

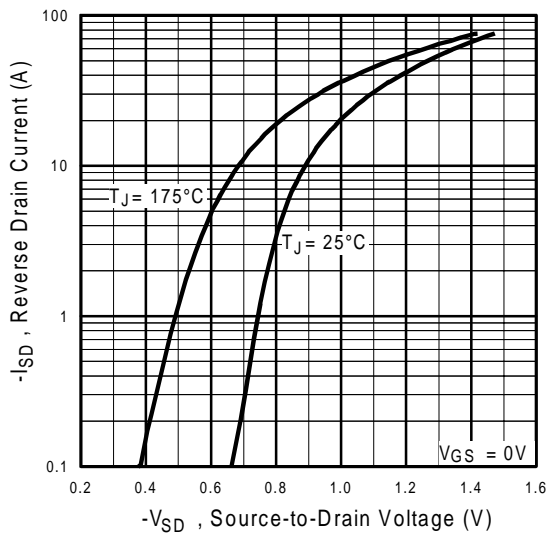


Fig 7. Typical Source-Drain Diode Forward Voltage

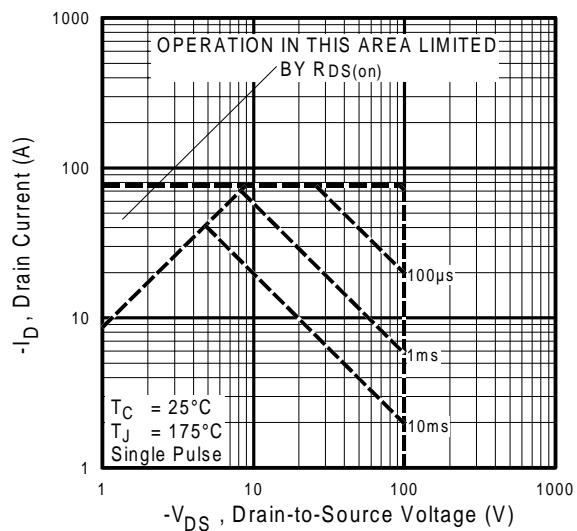


Fig 8. Maximum Safe Operating Area

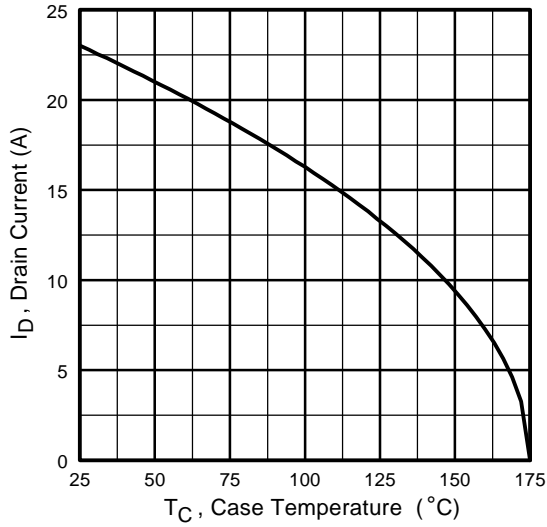


Fig 9. Maximum Drain Current Vs. Case Temperature

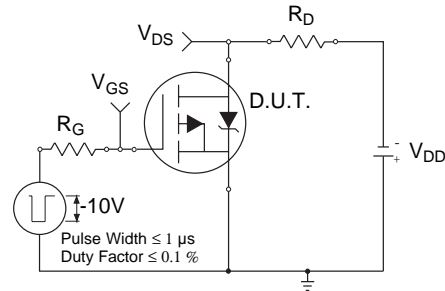


Fig 10a. Switching Time Test Circuit

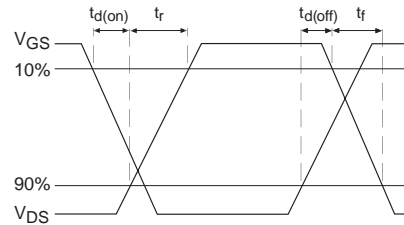


Fig 10b. Switching Time Waveforms

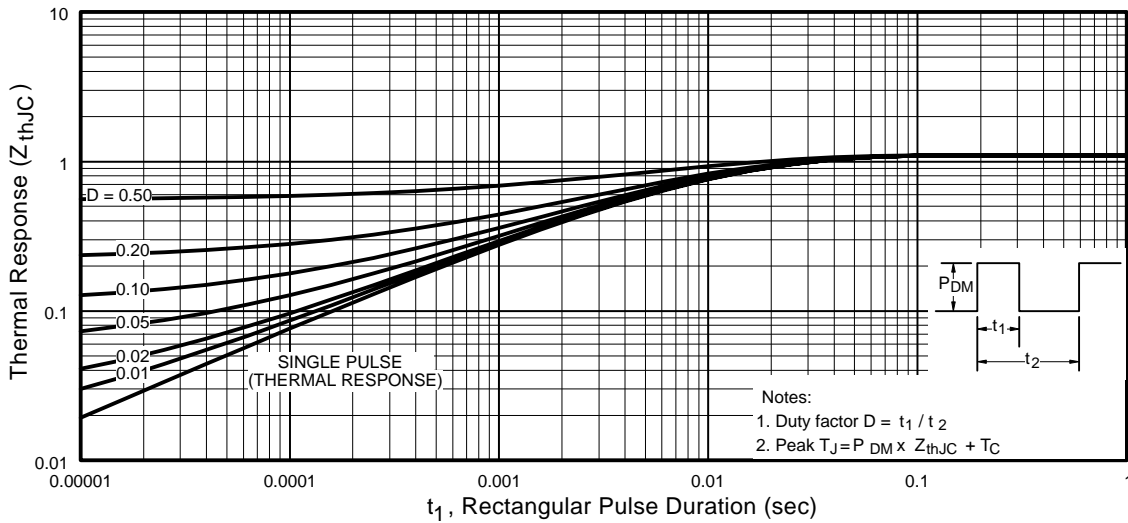


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

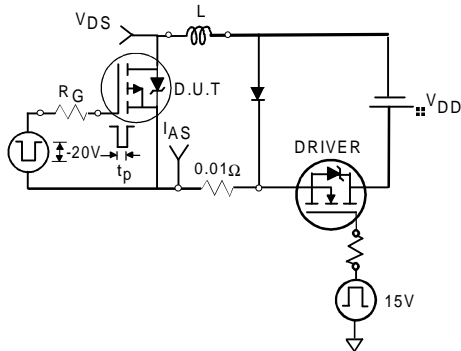


Fig 12a. Unclamped Inductive Test Circuit

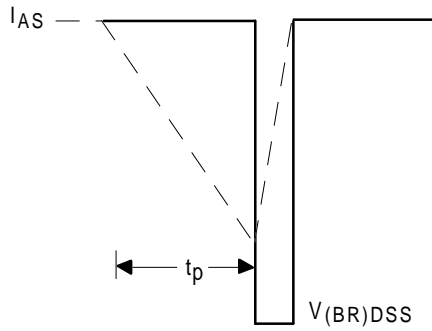


Fig 12b. Unclamped Inductive Waveforms

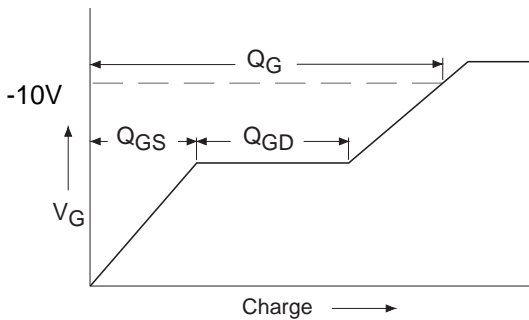


Fig 13a. Basic Gate Charge Waveform

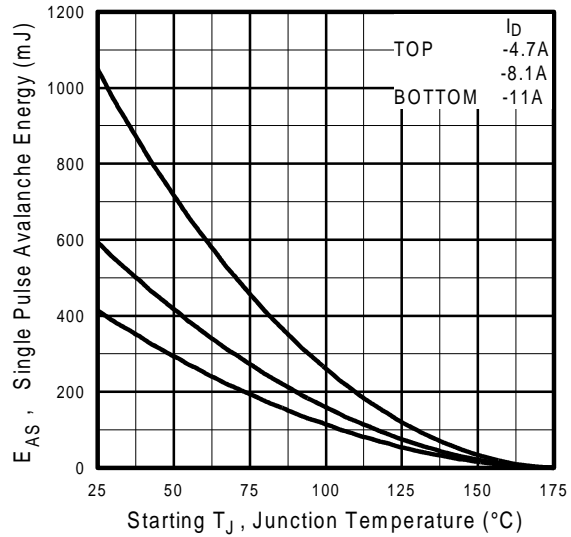


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

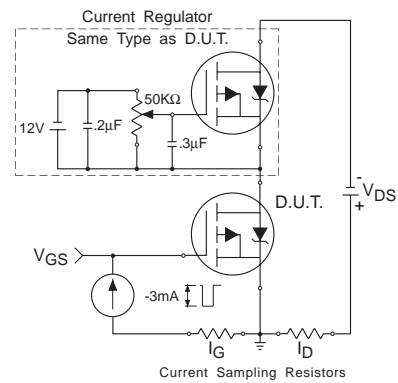
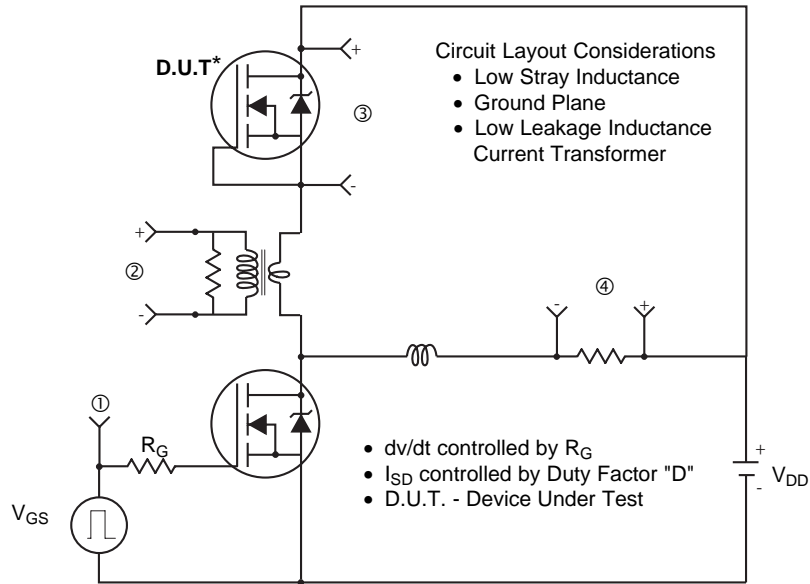
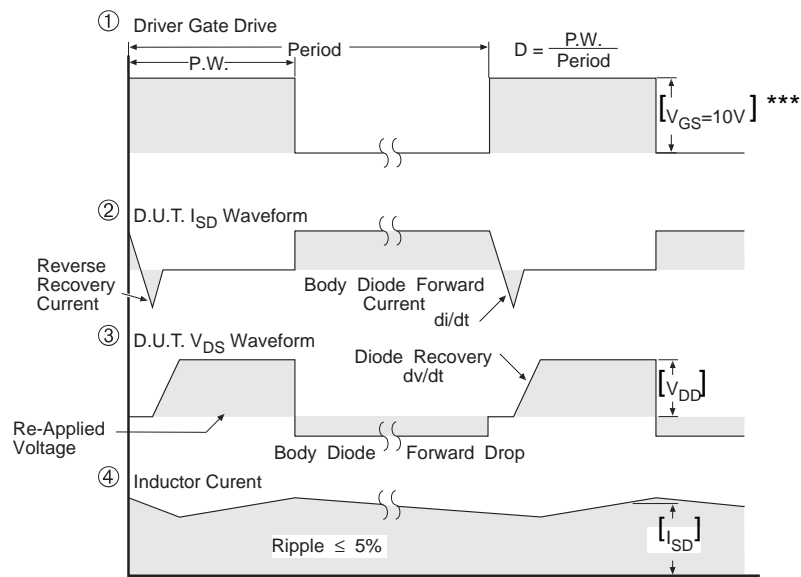


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

